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Posedge-One SPARTAN-6 FPGA Development Board
Rev 1.1

SPARTAN-6 LX 9 FPGA
On-Board USB-JTAG Programmer
512 KB SRAM Memory
USB-FIFO Interface (Up to 10 MB/s transfer speed)
64 Mbit QSPI Flash
48 User I/O

Title *Posedge-One SPARTAN-6 Development Board*			*www.posedge.ir* *Rayan-Sanat Tech.* *Isfahan Science and Technology Town, Isfahan* *Islamic Repuplic of IRAN*
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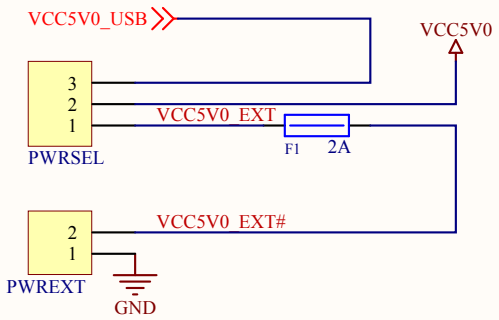
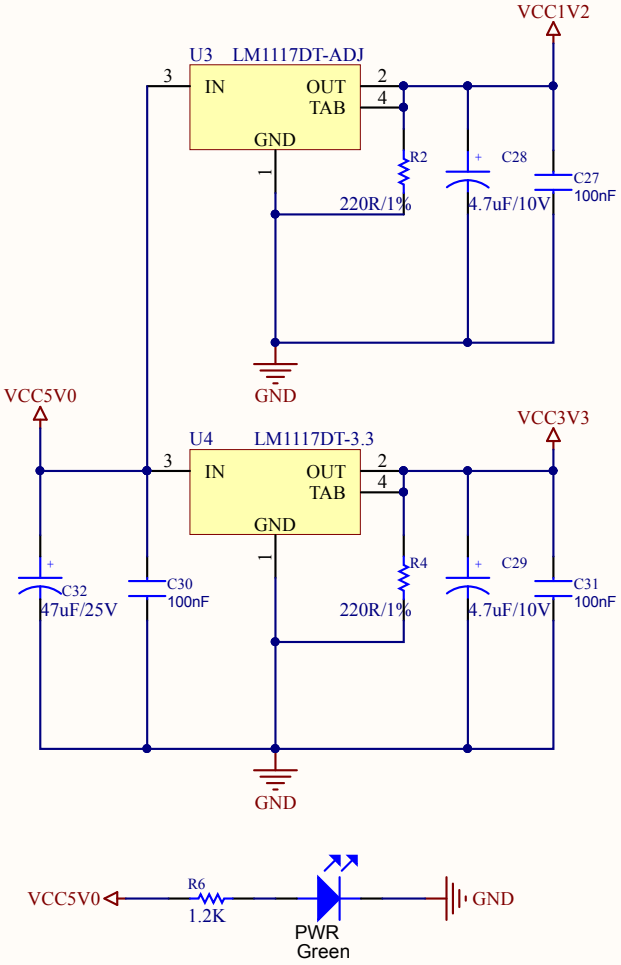
POWER





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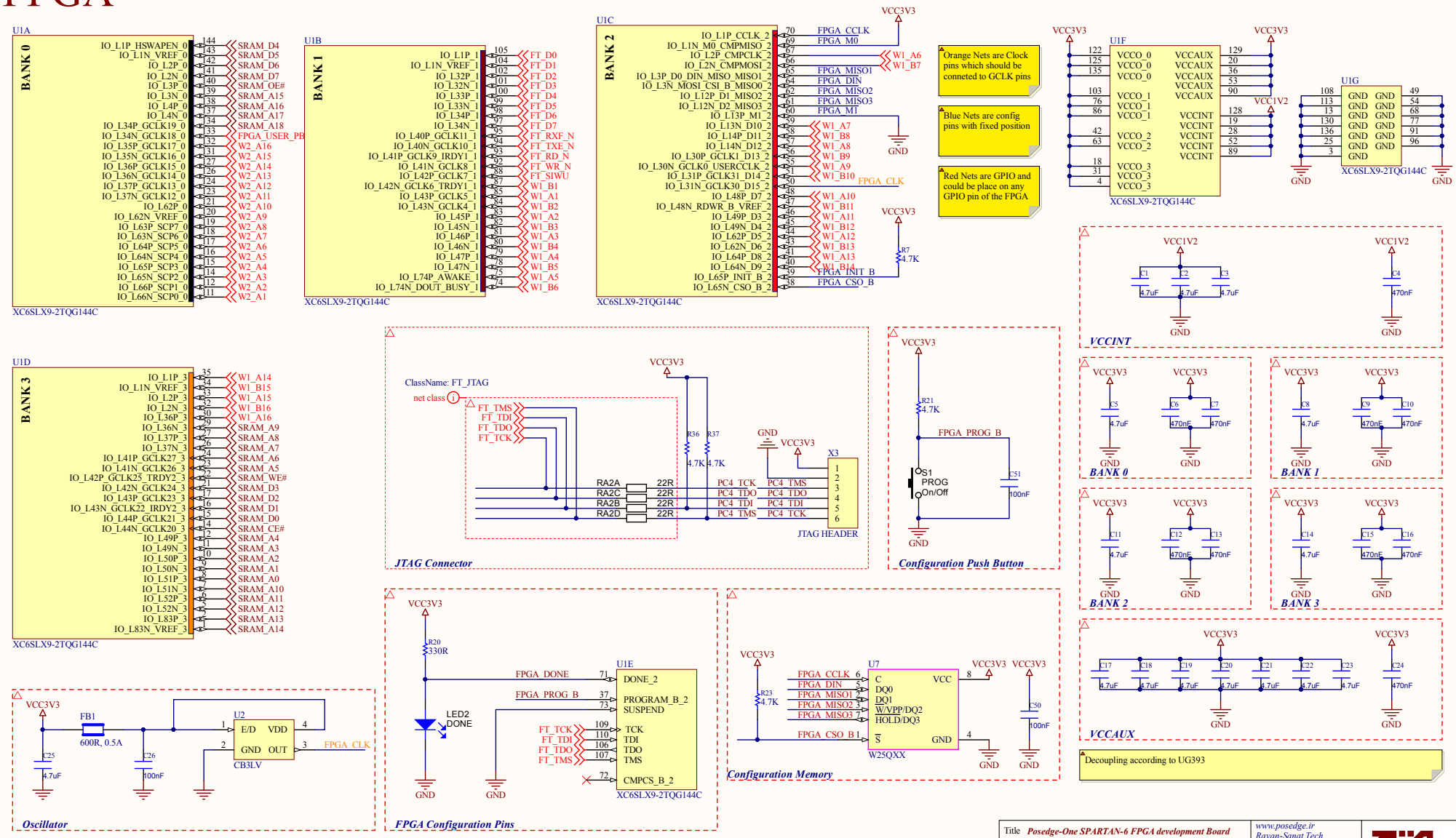
FPGA


U1A
BANK 0
IO_L1P_HSWAPEN_0
IO_L1N_VREF_0
IO_L2P_0
IO_L2N_0
IO_L3P_0
IO_L3N_0
IO_L4P_0
IO_L4N_0
IO_L34P_GCLK19_0
IO_L34N_GCLK18_0
IO_L35P_GCLK17_0
IO_L35N_GCLK16_0
IO_L36P_GCLK15_0
IO_L36N_GCLK14_0
IO_L37P_GCLK13_0
IO_L37N_GCLK12_0
IO_L62P_0
IO_L62N_VREF_0
IO_L63P_SCP7_0
IO_L63N_SCP6_0
IO_L64P_SCP5_0
IO_L64N_SCP4_0
IO_L65P_SCP3_0
IO_L65N_SCP2_0
IO_L66P_SCP1_0
IO_L66N_SCP0_0
SRAM_D4
SRAM_D5
SRAM_D6
SRAM_D7
SRAM_OE#
SRAM_A15
SRAM_A16
SRAM_A17
SRAM_A18
FPGA_USER_PB
W2_A16
W2_A15
W2_A14
W2_A13
W2_A12
W2_A11
W2_A10
W2_A9
W2_A8
W2_A7
W2_A6
W2_A5
W2_A4
W2_A3
W2_A2
W2_A1
XC6SLX9-2TQG144C
U1B
BANK 1
IO_L1P_1
IO_L1N_VREF_1
IO_L32P_1
IO_L32N_1
IO_L33P_1
IO_L33N_1
IO_L34P_1
IO_L34N_1
IO_L40P_GCLK11_1
IO_L40N_GCLK10_1
IO_L41P_GCLK9_IRDY1_1
IO_L41N_GCLK8_1
IO_L42P_GCLK7_1
IO_L42N_GCLK6_TRDY1_1
IO_L43P_GCLK5_1
IO_L43N_GCLK4_1
IO_L45P_1
IO_L45N_1
IO_L46P_1
IO_L46N_1
IO_L47P_1
IO_L47N_1
IO_L74P_AWAKE_1
IO_L74N_DOUT_BUSY_1
FT_D0
FT_D1
FT_D2
FT_D3
FT_D4
FT_D5
FT_D6
FT_D7
FT_RXF_N
FT_TXE_N
FT_RD_N
FT_WR_N
FT_SIWU
W1_B1
W1_A1
W1_B2
W1_A2
W1_B3
W1_A3
W1_B4
W1_A4
W1_B5
W1_A5
W1_B6
XC6SLX9-2TQG144C
U1C
BANK 2
IO_L1P_CCLK_2
IO_L1N_M0_CMPMISO_2
IO_L2P_CMPCLK_2
IO_L2N_CMPMOSI_2
IO_L3P_D0_DIN_MISO_MISO1_2
IO_L3N_MOSI_CSI_B_MISO0_2
IO_L12P_D1_MISO2_2
IO_L12N_D2_MISO3_2
IO_L13P_M1_2
IO_L13N_D10_2
IO_L14P_D11_2
IO_L14N_D12_2
IO_L30P_GCLK1_D13_2
IO_L30N_GCLK0_USERCCLK_2
IO_L31P_GCLK31_D14_2
IO_L31N_GCLK30_D15_2
IO_L48P_D7_2
IO_L48N_RDWR_B_VREF_2
IO_L49P_D3_2
IO_L49N_D4_2
IO_L62P_D5_2
IO_L62N_D6_2
IO_L64P_D8_2
IO_L64N_D9_2
IO_L65P_INIT_B_2
IO_L65N_CSO_B_2
FPGA_CCLK
FPGA_M0
W1_A6
W1_B7
FPGA_MISO1
FPGA_DIN
FPGA_MISO2
FPGA_MISO3
FPGA_MT
W1_A7
W1_B8
W1_A8
W1_B9
W1_A9
W1_B10
FPGA_CLK
W1_A10
W1_B11
W1_A11
W1_B12
W1_A12
W1_B13
W1_A13
W1_B14
FPGA_INIT_B
FPGA_CSO_B
VCC3V3
R7
4.7K
GND
XC6SLX9-2TQG144C
Orange Nets are Clock pins which should be conneted to GCLK pins
Blue Nets are config pins with fixed position
Red Nets are GPIO and could be place on any GPIO pin of the FPGA
U1F
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCAUX
VCCINT
VCC1V2
XC6SLX9-2TQG144C
U1G
GND
XC6SLX9-2TQG144C
U1D
BANK 3
IO_L1P_3
IO_L1N_VREF_3
IO_L2P_3
IO_L2N_3
IO_L36P_3
IO_L36N_3
IO_L37P_3
IO_L37N_3
IO_L41P_GCLK27_3
IO_L41N_GCLK26_3
IO_L42P_GCLK25_TRDY2_3
IO_L42N_GCLK24_3
IO_L43P_GCLK23_3
IO_L43N_GCLK22_IRDY2_3
IO_L44P_GCLK21_3
IO_L44N_GCLK20_3
IO_L49P_3
IO_L49N_3
IO_L50P_3
IO_L50N_3
IO_L51P_3
IO_L51N_3
IO_L52P_3
IO_L52N_3
IO_L83P_3
IO_L83N_VREF_3
W1_A14
W1_B15
W1_A15
W1_B16
W1_A16
SRAM_A9
SRAM_A8
SRAM_A7
SRAM_A6
SRAM_A5
SRAM_WE#
SRAM_D3
SRAM_D2
SRAM_D1
SRAM_D0
SRAM_CE#
SRAM_A4
SRAM_A3
SRAM_A2
SRAM_A1
SRAM_A0
SRAM_A10
SRAM_A11
SRAM_A12
SRAM_A13
SRAM_A14
XC6SLX9-2TQG144C
ClassName: FT_JTAG
net class
FT_TMS
FT_TDI
FT_TDO
FT_TCK
R36
R37
4.7K
RA2A
RA2C
RA2B
RA2D
22R
PC4_TCK
PC4_TMS
PC4_TDO
PC4_TDI
X3
JTAG HEADER
JTAG Connector
R21
4.7K
FPGA_PROG_B
S1
PROG
On/Off
C51
100nF
Configuration Push Button
VCCINT
BANK 0
BANK 1
BANK 2
BANK 3
VCCAUX
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
4.7uF
470nF
Decoupling according to UG393
FB1
600R, 0.5A
C25
C26
U2
E/D
VDD
GND
OUT
CB3LV
FPGA_CLK
Oscillator
R20
330R
LED2
DONE
U1E
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
CMPCS_B_2
FPGA_DONE
FPGA_PROG_B
XC6SLX9-2TQG144C
FPGA Configuration Pins
R23
4.7K
U7
C
DQ0
DQ1
W/VPP/DQ2
HOLD/DQ3
S
VCC
W25QXX
C50
100nF
Configuration Memory
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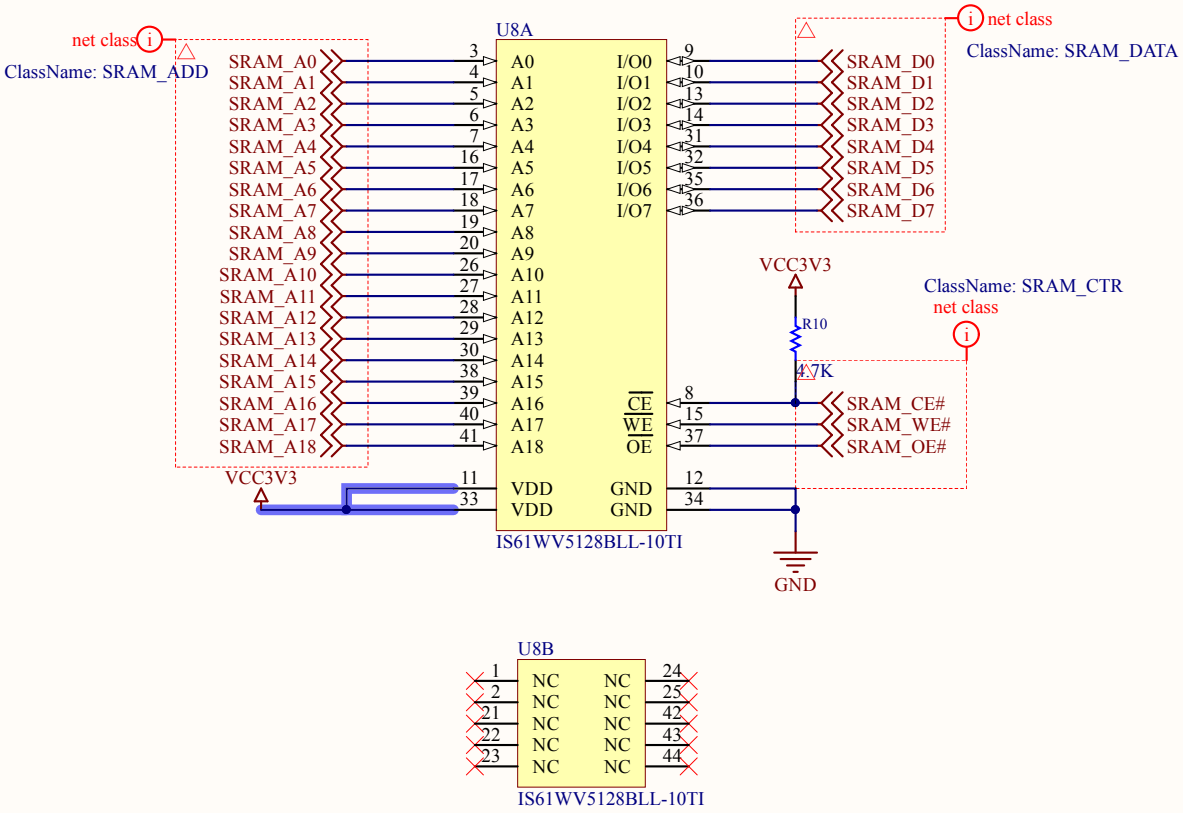
SRAM



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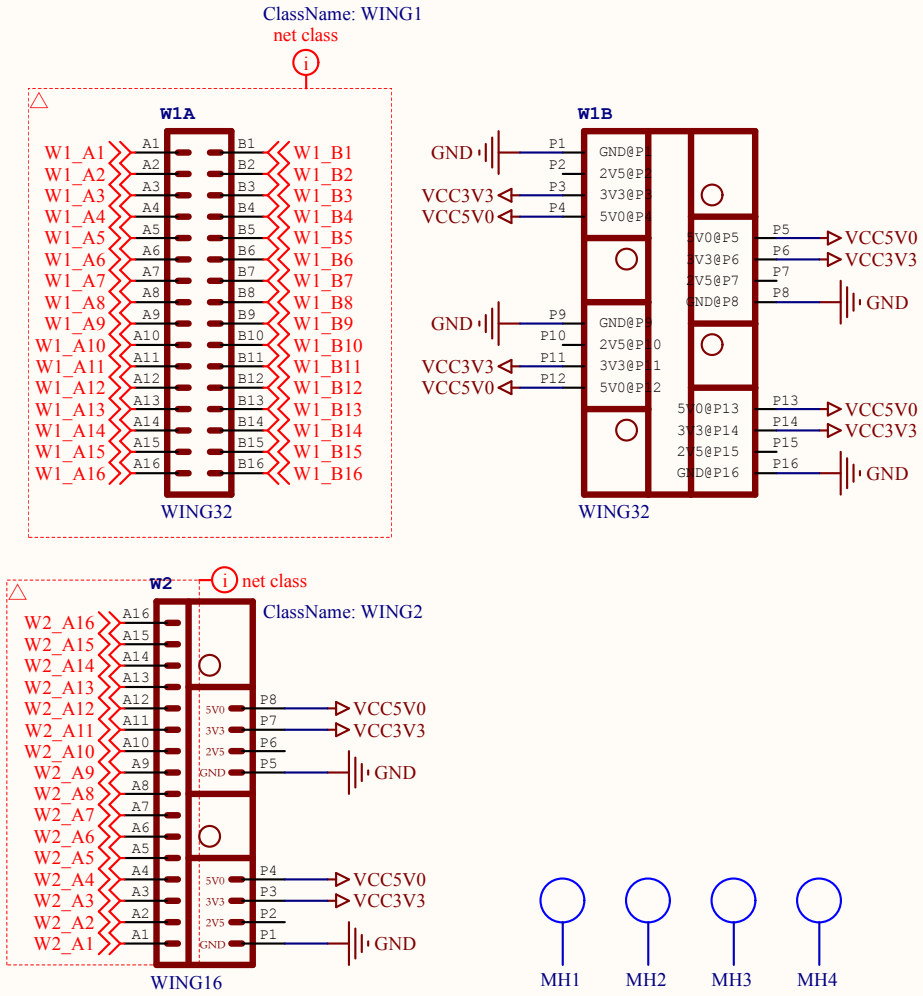
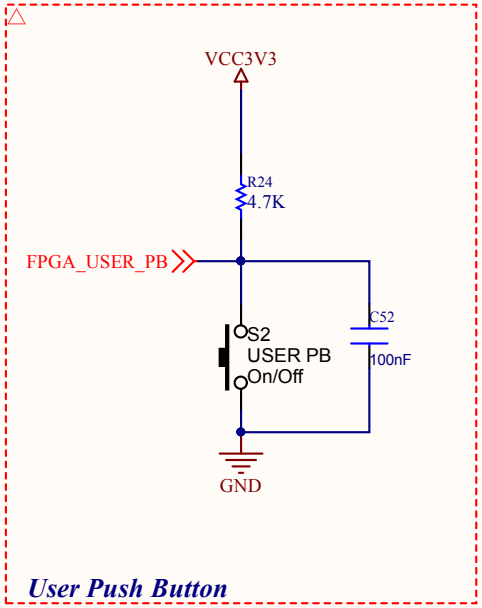
GPIO





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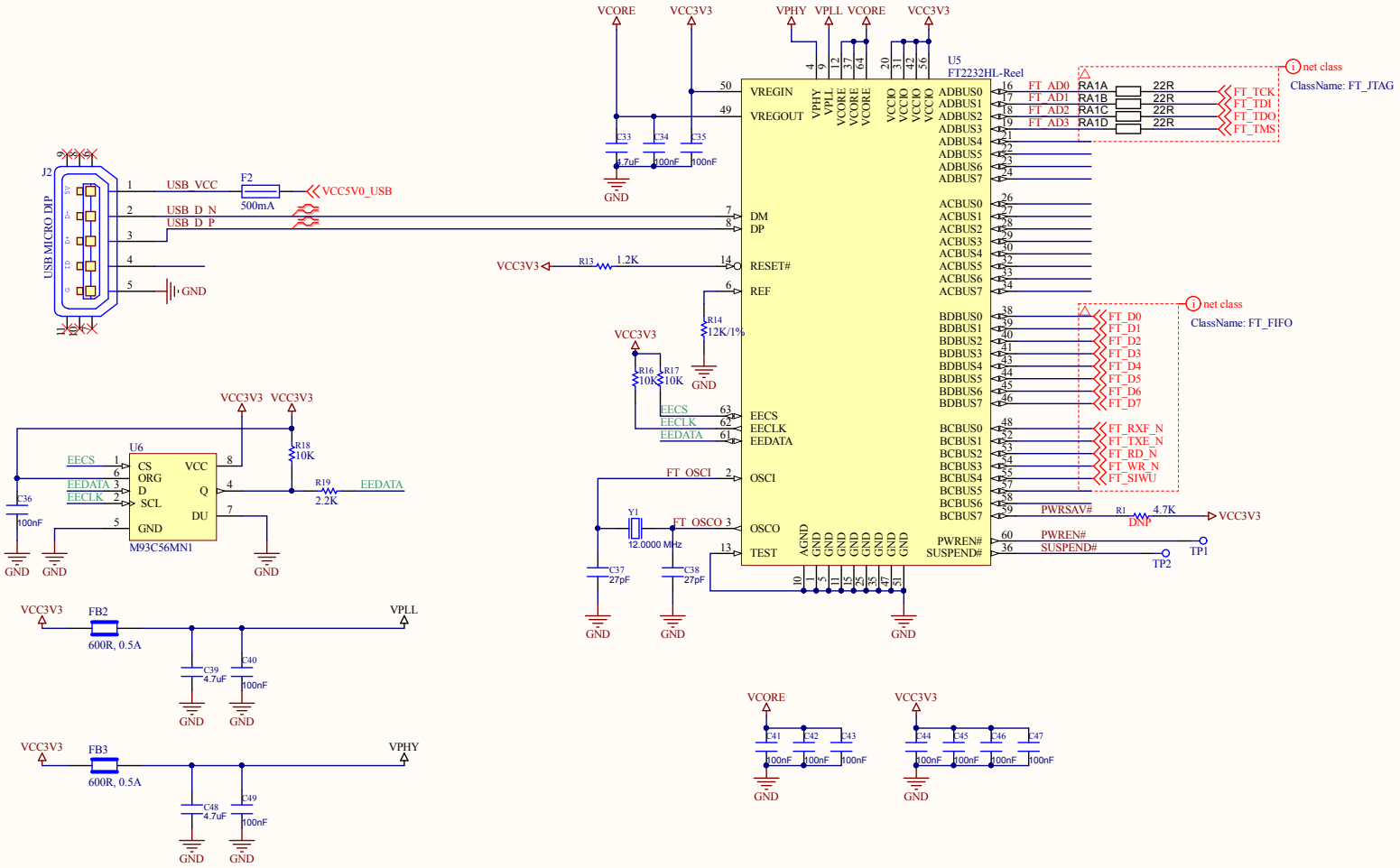
USB-JTAG



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